

**RKDF University, Bhopal**  
**Faculty Profile**



Basic Information				
<b>Name</b>	<b>Dr Sachin Bandewar</b>			
<b>Date of Birth</b>	<b>01-11-1987</b>			
<b>Designation</b>	<b>Assistant Professor</b>			
<b>Department</b>	<b>Electronic &amp; Communication Engineering</b>			
<b>Experience</b>	<b>15 Years</b>			
<b>Email ID</b>	<b>sachin.bandewar9@gmail.com</b>			
<b>Contact No</b>	<b>9977183247</b>			
Educational Qualifications				
Description	Year	%	Institute/University	
UG-B.E. (Electronic & Communication Engineering)	2009	66.38	RGPV BHOPAL	
PG-1 M. Tech. (Energy Technology)	2012	74.80	RGPV BHOPAL	
PG-2 M. Tech. (Digital Communication)	2015	79.80	RGPV BHOPAL	
(Ph. D.) Engineering and Technology	2024		RKDF UNIVERSITY	
Post Doctorate	-	--	-	
NET Qualified/GATE	-	-	-	
Experience Detail				
Experience (Teaching/Research )	Designation	Duration		Name of Institute/University
		From	To	
<b>Teaching</b>	Lecture	22-Feb-2010	20-Sept-2012	<b>Sri Satya Sai College of Engineering Bhopal (M.P.)</b>
<b>Teaching and Research</b>	Assistant Professor	21-Sept-2012	Till date	<b>Sri Satya Sai College of Engineering RKDF University Bhopal (M.P.)</b>
Publications				
<b>No. of Papers Published (Attach Annexure    20</b> <b>of papers published in peer-reviewed or</b> <b>refereed journals)</b>				

<b>No. of Books Published</b>	-		
<b>Books Chapters Published (Provide print of 1<sup>st</sup> Page of Book</b>	-		
No. of Patents Published/Grant	<b>01</b>		
<b>Ph. D/M. Phil Project supervised</b>			
<b>Research Program</b>	<b>Award</b>	<b>Under Supervision</b>	<b>Name of University</b>
<b>Ph. D (Provide detail i.e. name, title etc)</b>	-	-	-
<b>M. Phil</b>	-	-	-
<b>PG Thesis/Dissertation</b>	21	02	<b>RKDF UNIVERSITY, BHOPAL</b>
<b>Area of Expertise (100 words)</b>			
Enrich experience of more than 15+ years in Education sector. Proficient in Data analysis, process reengineering and documentation and research project activities, Helpdesk Management, Training, workshop etc. Area of Expertise in Drone technology. Antenna design VLSI and Digital communication.			
<b>Award and Achievement</b>			
<b>Name of Award</b>	<b>Description (With certified of Copy award)</b>		
<b>National</b>	-		
<b>International</b>	-		
<b>Conference/Seminar/Workshops/FDP</b>			
<b>Description</b>	<b>No.</b>		
<b>Conference/Seminar paper presentation</b>	<b>02</b>		
<b>Conference/Seminar attended/ organized</b>	-		
<b>Work shop attended/ organized</b>	<b>02</b>		
<b>FDP Attended/ organized</b>	<b>01</b>		
<b>Research Project</b>			
<b>Name of Project</b>	<b>Funding Agencies</b>	<b>Amount</b>	
-	-	-	

- **Any other Achievement**



## List of publications

- [01] Khushboo Ahirwar, Sachin Bandewar, Anand Kumar Singh, (Feb 2014) "FPGA Implementation ALU Based on Reversible Logic" international journal of engineering sciences & research technology volume:1 issue:01. pp:811-814  
<https://www.ijert.org/research/fpga-implementation-alu-based-on-reversible-logic-IJERTV3IS10818.pdf>
- [02] Amrita Shrivastava, Subhasis Bose, Sachin Bandewar, (June 2014) "Performance Analysis of and Delay Estimation on the RC Delay MOSFET Model" International Journal of Engineering and Management Research (IJEMR). Volume 04: issue03.pp:134-137  
<https://ijarce.com/wp-content/uploads/2012/03/IJARCE61-a-Amrita-Shrivastava-performance.pdf>
- [03] Amreen Parveen, Sachin Bandewar, Anand Kumar Singh, (June 2014) "Frequency Divider Digital CMOS Parallel Counter Using Pass Transistor Logic" International Journal of Electronics Communication and Computer Engineering. Volume 05: issue01.pp:109-113  
[https://ijecce.org/administrator/components/com\\_jresearch/files/publications/IJECCE\\_2328\\_Final.pdf](https://ijecce.org/administrator/components/com_jresearch/files/publications/IJECCE_2328_Final.pdf)
- [04] Sachin bandewar, Mala Kushwaha, Shweta Raghuvanshi, (June 2014) "metastability errors in CMOS interface circuits" international journal of advanced research in computer science and electronics engineering (IJARCSEE). Volume 02: issue05.pp:462-467  
<https://www.semanticscholar.org/paper/METASTABILITY-ERRORS-IN-CMOS-INTERFACE-CIRCUITS-Bandewar-Kushwaha/52c2dbfe6c2738b85056099f55bdeace6028d487#paper-topics>
- [05] Jyoti Tiwari, Sachin bandewar, (November 2015) "To Reduce leakage power of CMOS logic circuit through lector technique" International Journal of Emerging Technology and Advanced Engineering. Volume:5 issue:11. pp:261-269  
[https://www.ijetae.com/files/Volume5Issue11/IJETAE\\_1115\\_46.pdf](https://www.ijetae.com/files/Volume5Issue11/IJETAE_1115_46.pdf)
- [06] Dhyandendra Singh Chandel, Sachin Bandewar, Anand Kumar Singh, (July 2015) "Low Power 10T XOR based 1 Bit Full Adder" International Journal of Computer Applications Volume:121 issue:01. pp:13-16 <https://research.ijcaonline.org/volume121/number1/pxc3904019.pdf>
- [07] Ambresh Patel, Anand Kumar Singh, Sachin Bandewar, (may 2015) "CMOS Layout Design and Performance Analysis for Synchronization Failures using 50nm Technology" International Journal of Computer Applications (0975 – 8887) Volume 117 issue11.pp:33-37  
<https://research.ijcaonline.org/volume117/number11/pxc3903200.pdf>
- [08] Amrita Shrivastava, Subhasis Bose, Sachin Bandewar, (may 2015) "Performance Analysis of and Delay Estimation on the RC Delay MOSFET Model" International Journal of Engineering and Management Research (IJEMR). Volume 04: issue03.pp:134-137  
<https://www.indianjournals.com/ijor.aspx?target=ijor:ijemr&volume=4&issue=3&article=026>
- [09] Dhyandendra Singh Chandel, Sachin Bandewar, Anand Kumar Singh, (June 2015) "Low Power-Area Efficient 1bit Full Adder with Modified Gated Diffusion Input Technique" **International Journal of Engineering Trends and Technology (IJETT)** Volume:24 issue:04. pp:165-168  
<https://studylib.net/doc/12913611/low-power-area-efficient-1bit-full-adder-with-modified-gated>
- [10] Vishal Joshi, Sachin Bandewar, (2015) "To Reduce the Number of Flip-Flops by Using State Look-Ahead Logic Based on Parallel Counter" INTERNATIONAL JOURNAL OF SCIENTIFIC PROGRESS AND RESEARCH (IJSR) Volume:16 issue:01. pp:10-15 ISSN: 2349-4689  
[https://www.ijspr.com/citations/v16n1/IJSR\\_1601\\_103.pdf](https://www.ijspr.com/citations/v16n1/IJSR_1601_103.pdf)
- [11] Braj Kishor, Anand Kumar Singh, Sachin Bandewar, (2015) "Implementation of Trinary/Quaternary Addition using Multivalued Logic Digital Circuit" International Journal of Computer Applications (0975 – 8887) Volume 118 – No. 4, May 2015  
<https://research.ijcaonline.org/volume118/number4/pxc3903114.pdf>
- [12] Parvin Akhtar, Sachin bandewar, (Aug 2016)"logarithmic multiplier using seamless pipelined" international journal of latest research in engineering and technology, volume no 2 Issue no 8, pp: 76-81  
[https://archive.org/details/Httpwww.ijer.inijerpublicationv5s8IJER\\_2016\\_817.pdf](https://archive.org/details/Httpwww.ijer.inijerpublicationv5s8IJER_2016_817.pdf)
- [13] Mayura Upasani, Sachin Bandewar, (November 02,2016)"To Improve Noise by Increasing the Output Current for Dynamic CMOS Logic With Stack Technique " International Journal of

Innovative Trends in Engineering (IJITE), VOL-18,  
[https://www.ijite.com/citations/IJITE\\_18021004.pdf](https://www.ijite.com/citations/IJITE_18021004.pdf)

[14] Mayura Upasani, Sachin Bandewar, (july-2016)"To Improve Noise by Reducing Rise Time, Fall Time for Dynamic CMOS Logic With Stack Technique " International Journal of Emerging Technology and Advanced Engineering (IJETA), Volume-6, Issue-11,  
[https://www.ijetae.com/files/Volume6Issue7/IJETA\\_0716\\_09.pdf](https://www.ijetae.com/files/Volume6Issue7/IJETA_0716_09.pdf)

[15] Parvin Akthar, Sachin bandewar, (Aug 2016) "logarithmic multiplier an analytical review" international journal of engineering research. Volume:5 issue:8. pp:721-723  
<https://www.semanticscholar.org/paper/Logarithmic-Multiplier%3A-An-Analytical-Review-Akhter-Bandewar/b23f99825ed647115cdac594cb0f056991e04d33>

[16] Sachin bandewar, Virendra Singh Chaudhary, (June-2022) "SMART ANTENNA DESIGN FOR MOBILE APPLICATION." i-Manager's Journal on Mobile Applications & Technologies, 2022, Vol 9, Issue 2, p7. ISSN: 2350-1413  
<https://doi.org/10.26634/jmt.9.2.19065>

[17] Sachin bandewar, Virendra Singh Chaudhary, (2023) "Design and Analysis of Smart Antenna for Mobile Application" SAMRIDDHI: A Journal of Physical Sciences, Engineering and Technology, Vol 15 No 01 (2023). ISSN: 2023-01-30  
<https://doi.org/10.18090/10.18090/samriddhi.v15i01.19>

[18] Deepak Giri, Sachin bandewar, (2023) "A Comprehensive Review of Approximate Multipliers in Power Efficient Computing: SHODH SANGAM -- A RKDF University Journal of Science and Engineering, Vol 06 No 03 (2023). ISSN: 2581-5806  
[http://shodhsangam.rkdfuniv.in/Content/Documents/papers/Deepak\\_5640.pdf](http://shodhsangam.rkdfuniv.in/Content/Documents/papers/Deepak_5640.pdf)

[19] Sachin bandewar, Virendra Singh Chaudhary, (2024) "Optimal direction of arrival estimation for digital beamforming using machine learning" Journal of Integrated Science and Technology, Vol 12 No 03. <https://pubs.thesciencein.org/journal/index.php/jist/article/view/a771/498>